EMULATOR CHIP/BOARD ARCHITECTURE AND INTERFACE

ABSTRACT OF THE DISCLOSURE

A communication interface for an in-circuit emulation system. The interface uses four pins between a virtual microcontroller (an FPGA emulating a microcontroller) and a real microcontroller under test. The bus is fast enough to allow the two devices to operate in synchronization. I/O reads, interrupt vector information and watchdog information is provided over the bus in a time fast enough to allow execution in lock step. Two data lines are provided, one is bi-directional and one is driven only by the microcontroller. A system clock is provided and the microcontroller supplies its clock signal to the FPGA since the microcontroller can operate at varying clock speeds. The bus is time-dependent so more information can be placed on this reduced-pin count bus. Therefore, instructions and data are distinguished based on the time the information is sent within the sequence. The bus can be used to carry trace information, program the flash memory on the microcontroller, perform test control functions, etc.